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patent attorneys

August 14, 2003

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on August 14, 2003.

Date of Signature:

P.O. Box 1450 Alexandria, VA 22313-1450

Re:

Commissioner for Patents

U.S. Patent Application Serial No. 10/615,100 for

VITERBI DECODER Our Ref. No. 1406/153

Sir:

Please find enclosed in connection with the subject U.S. patent application the following documents:

- 1. Information Disclosure Statement (1 page);
- 2. Form PTO-1449 (1 page) in duplicate;
- 3. Copies of cited references (7 references); and
- 4. A return-receipt postcard to be returned to us with the U.S. Patent and Trademark Office filing stamp thereon.

The Commissioner is hereby authorized to charge any fees associated with the filing of this correspondence to Deposit Account No. 50-0426.

Respectfully submitted,

JENKINS, WILSON & TAYLOR, P.A.

Richard E. Jenkins

Registration No. 28,428

REJ/gwc **Enclosures** 

Customer No. 25297



I hereby cerify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandra, VA 22313-1450 on August 14, 2003

Gayle W. Chaney
Date of Signature

S-1403

PATENT

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Mario Traeber

Group Art Unit: Not Assigned

Serial No.: 10/615,100

Examiner: Not Assigned

Filed: July 8, 2003

Docket No.: 1406/153

Confirmation No.: Not Assigned

For: VITERBI DECODER

## INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

In accordance with 37 C.F.R. 1.56, 1.97, and 1.98, applicants' undersigned attorney brings to the attention of the Patent and Trademark Office the documents listed on the attached form PTO-1449. Copies of the references as well as Form PTO-1449 are attached hereto. This is not to be construed as a representation that a search has been made or that a reference is relevant merely because cited.

Early passage of the subject application to issue is earnestly solicited.

Although it is believed that no fee is due, the Commissioner is hereby authorized to charge any fees associated with the filing of this Information Disclosure Statement to Deposit Account No. 50-0426.

Respectfully submitted,

JENKINS, WILSON & TAYLOR, P.A.

Date: 6-14-03

By:

Richard E. Jenkins
Registration No. 28,428

REJ/gwc

Enclosures

Customer No. 25297

FORM PTO-1449 U.S. Department of Commerce					Attorney Docket No. 1406/153			Serial No.
Patent and Trademark Office								10/615,100
tint of Door	ta Cito	d by Applicant						
List of Docum	nents Cite	d by Applicant						
	· 45/1				Applicant(s): Mario Traeber			
AUG 1 B	MIG 1 8 2003 E				Filing Date: July 8, 2003			Group
U.S. PATENT DOCUMENTS								
Examiner Initial		Document Number	Date	Name		Class	Subclass	Filing date if Appropriate
	1.	6,209,209 B1	03/27/2001	Hori et al.				
<b>.</b>		L	FOREIGN PA	ATENT	DOCUMEN	TS		
		Document	Date	Country		Name of Patentee or		Translation
		Number			Applicant		Yes   No	
	2.	197 42 958 A1	04/29/1999	Germa	ny	Siemens AG		No
	3.	2000 059 238	02/25/2000	Japan		Mitsubishi Electric Corp.		Yes
				(Abstract Only)				(Abstract Only)
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)							.)	
	4.	Shafiee, H. et al., "A Reduced-Complexity Trellis Search Decoding Algorithm for Extended Class IV Partial Response Systems," <u>IEEE International Conference on Communications</u> , Vol. 4, pp. 120-124 (June 14, 1992).						
	5.	Shieh, Ming-Der et al., "Efficient Management of In-Place Path Metric Update And Its Implementation for Viterbi Decoders," IEEE International Symposium on Circuits and Systems, Vol. 4, pp. 449-452 (May 31, 1998).						
	6.	Shung, C. Bernard et al., "VLSI Architectures for Metric Normalization in the Viterbi Algorithm," IEEE International Conference on Communications, Vol. 4, pp. 1723-1728 (April 15, 1990).						
	7.	Tsui, Chi-ying et al., "Low Power ACS Unit Design for the Viterbi Decoder," IEEE International Symposium on Circuits and Systems, pp. 137-140 (May 30, 1999).						

EXAMINER	DATE CONSIDERED
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<sup>\*</sup>Examiner Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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FORM PTO-1449 U.S. Department of Commerce Patent and Trademark Office				Attorney Docket No. 1406/153			Serial No. 10/615,100	
List of Docum	ents Cite	ed by Applicant						
OIPER				Applicant(s): Mario Traeber				
AUG 1	8 2003				Filing Dat	e: July 8,	2003	Group
AUG TRAO	EMARKO		U.S. PAT	ENT DO	CUMENTS	S		
Examiner Initial	ıminer Document Da		Date	Name		Class	Subclass	Filing date if Appropriate
	1.	6,209,209 B1	03/27/2001	Hori et	al.			
			FOREIGN P	ATENT	DOCUME	NTS		
		Document Number	Date	Country		Name of Patentee or Applicant		Translation Yes   No
	2.	197 42 958 A1	04/29/1999	Germany		Siemens AG		No
	3.	2000 059 238	02/25/2000	Japan		Mitsubishi Electric Corp.		Yes (Abstract Only)
	ТО	HER DOCUMEN	NTS (Includino	g Author	, Title, Date	e, Pertinen	t Pages, Etc	.)
	4.	Shafiee, H. et al. Class IV Partial I Vol. 4, pp. 120-1	Response Syst	ems," <u>IE</u>				
	5.	Shieh, Ming-Der et al., "Efficient Management of In-Place Path Metric Update And Its Implementation for Viterbi Decoders," IEEE International Symposium on Circuits and Systems, Vol. 4, pp. 449-452 (May 31, 1998).						
	6.	Shung, C. Bernard et al., "VLSI Architectures for Metric Normalization in the Viterbi Algorithm, IEEE International Conference on Communications, Vol. 4, pp. 1723-1728 (April 15, 1990).						
	7.	Tsui, Chi-ying et Symposium on C						EEE International

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